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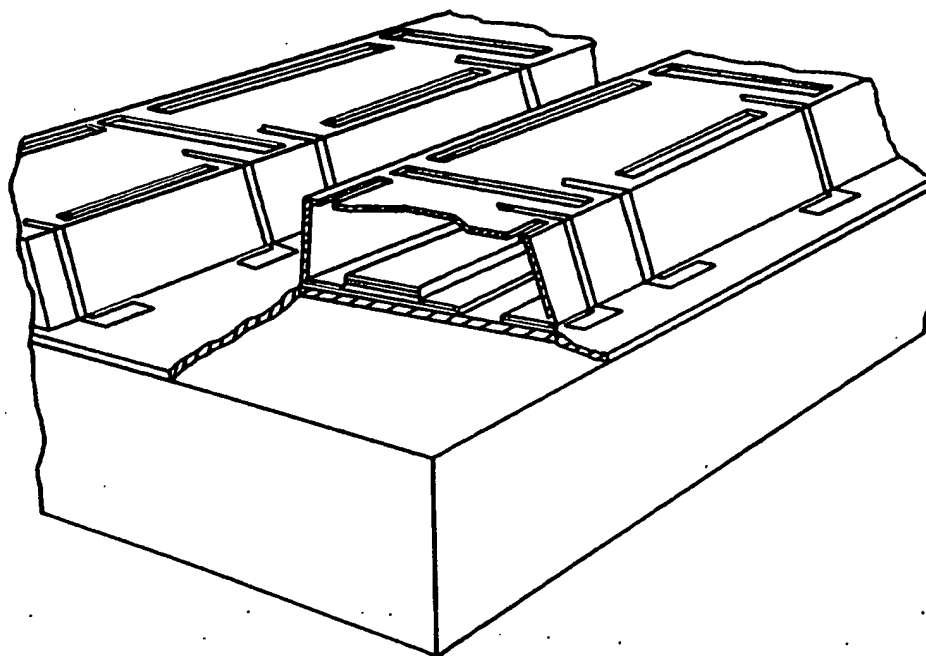
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(54) Title: TWO-LEVEL MICROBRIDGE BOLOMETER IMAGING ARRAY AND METHOD OF MAKING SAME



(57) Abstract

A two-level IR detector imaging array of high fill-factor design. The upper microbridge detector level is spaced above and overlies the integrated circuit and bus lines on the substrate surface below.

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## TWO-LEVEL MICROBRIDGE BOLOMETER IMAGING ARRAY AND METHOD OF MAKING SAME

### FIELD OF THE INVENTION

The field of the invention is in a two-level infrared bolometer array based on a pitless microbridge detector structure with integrated circuitry on a silicon substrate beneath.

### BACKGROUND AND SUMMARY OF THE INVENTION

This invention is directed to a pixel size sensor of an array of sensors for an infrared pitless microbridge construction of high fill factor. In this invention the large fill factor ( $> 75\%$ ) is made possible by placing the detector microbridge on a second plane above the silicon surface carrying the integrated diode and bus lines.

Prior art microbridge thermal detector arrays in a silicon substrate have been fabricated and one such example is shown in the patent 3,801,949. In these prior art references, the small pixels have a low fill factor because the detector, the bus lines and the diode are all in the same plane, each using a substantial share of the available pixel area.

### BRIEF DESCRIPTION OF THE DRAWING

Figure 1 is an elevation view of the two-level detector.

Figure 3 is a plan view of the top plane of the detector.

Figure 3a shows adjoining detectors.

Figure 4 is a schematic representation of a pixel circuit and connections.

Figure 5 and 6 show perspective and top views of an array of the two-level detectors.

### DESCRIPTION

The elevation and/or cross section view of the two-level pitless microbridge bolometer pixel 10 is shown in Figure 1. The device 10 has two levels, an elevated microbridge detector 11 and lower level 12. The lower level has a flat surfaced semiconductor substrate 13, such as single crystal

silicon substrate. The surface 14 of the silicon substrate 13 has fabricated thereon several components of an integrated circuit 15 including diodes, x and y bus lines, connections, and contact pads at the ends of the x and y bus lines, the fabrication following conventional silicon IC technology. The integrated circuit 15 is coated with a protective layer of silicon nitride 16. A top plan view of the lower level is shown in Figure 2 and comprises a y-diode metal (via) and an x-diode metal (via), chrome-gold-chrome x and y bus lines, a y-side bus conductor contact 18, an x-side contact 19, and the silicon nitride protective layer. The valley strip 17 is the area not covered by the elevated detector.

Referring again to Figure 1, the elevated detector level 11 includes a silicon nitride layer 20, a serpentine metallic resistive layer 21, such as of nickel-iron, often called permalloy, a silicon nitride layer 22 over the layers 20 and 21, and an IR absorber coating 23 over the silicon nitride layer 22. The absorber coating may also be of a nickel-iron alloy. Downwardly extending silicon nitride layers 20' and 22' deposited at the same time during the fabrication make up the four sloping support legs for the elevated detector level. The number of support legs may be greater or less than four. The cavity 26 (approximately 3 microns high) between the two levels is ambient atmosphere. During the fabrication process, however, the cavity 26 was originally filled with a previously deposited layer of easily dissolvable glass or other dissolvable material until the layers 20, 20' and 22, 22' were deposited. Subsequently in the process the glass was dissolved out to leave the cavity. In Figure 1 the horizontal dimension, as shown, is greatly foreshortened for descriptive purposes. That is, the height of Figure 1 is greatly exaggerated in the drawing compared to the length in order to show the details of the invention.

Figure 3 is a top plan view of the elevated detector level 11. This drawing is made as though the overlying absorber coating 23 and upper silicon

nitride layer 22 are transparent so the serpentine resistive layer path 21 can be shown. The exact layout of the serpentine pattern 21 is not significant to the invention. The resistive lines and spaces may be about 1.5 micron. Permalloy was selected as the material for the resistive path 21 in one embodiment because of its relatively high resistivity together with a good temperature coefficient of resistance. In one embodiment the resistivity was on the order of 2500 ohms, with a fill factor of about 75%. The ends of the resistive paths 21a and 21b are continued down the slope area 30 to make electrical contact with pads 31 and 32 on the lower level.

Figure 3 also shows nitride window cuts 35, 36 and 37 which are opened through the silicon nitride layers 20 and 22 to provide access to the phos-glass beneath for dissolving it from beneath the detector plane. These nitride cuts may be made by ion milling or other suitable process. It may be noted that the ion milled cuts 35, 36 and 37 to provide this access are very narrow ( $< 2$  microns) and are shared with adjacent pixels on the sides, (see Figure 3a), thus maximizing the area available to the detector and thus maximizing the resulting fill-factor. The four supporting legs may be as short or as long as necessary to provide adequate support and thermal isolation. With the detector thickness of 3000A or less, the thermal impedance is high over the entire detector film. Consequently, short legs should not contribute excessively to the conductance. Figure 3a shows that the adjacent identical pixels are in close proximity.

Figure 4 is a schematic representation of a pixel circuit shown in the other figures comprising the sensing element 21 and the connections to it which are clearly labeled on the drawing.

Although the description has been basically in terms of individual detector pixels, the invention is directed to an x,y array assembly of adjoining pixels forming an imaging or mosaic detector array. Each pixel assembly may cover an area about 50 microns on a side, for example. Figures 5 and 6, as

well as Figure 3a show a section of the array. Figure 5 shows in perspective the sensing ridges of abutting sensors in a column. This figure is partially cut away to show the lower level and the cavity as well. The ridges may be about 40 microns wide, so that the elevated detector pixels 11 are on the order of 50x40 microns.

Figure 6 is a top view block diagram of Figure 5. In the operation of an array of this general type, a suitable IR lens system is usually used to focus a scene onto the array of pixels. A chopper may be used if desired to interrupt the incoming IR energy in synchronism with the related utilizing video electronics. The focused scene heats each pixel according to the energy of the received scene at each pixel position and changes the resistance of the resistive layer 21 according to the pixel temperature.

Further described below is a sequence of fabrication steps for the upper level. Following the deposition of the silicon nitride layer 16 in fabricating the lower level 12 and the cuts of the x-side contact area 19, the y-side busconductor contact area 18, the cuts of the x-pads and y-pads, the lower level of electronic components and conductors is complete. The construction of the upper level 11 is then ready to commence. A layer of phos-glass or other easily soluble material approximately 3 microns thick is deposited and delineated along x-direction strips and the strip slopes 30 and 30' are thoroughly rounded to eliminate slope coverage problems. In the delineation the glass is cut to less than one micron on the strip 17. The remaining glass is cut to open the strip, and the external glass areas including the x-pad and the y-pad. The upper plane silicon nitride base layer 20 is then deposited, the nickel-iron resistance layer 21 is deposited, delineated, and connected to the lower plan contacts 18 and 19, and covered with silicon nitride passivation layer 22. The trim site 40 (Figure 3) is cut, x-pads and y-pads are opened, the absorber coating 23 is deposited and delineated, and finally the side slots 35,

36 and 37 are ion milled allowing the phos-glass to be dissolved from beneath the detector plane.

The embodiments of the invention in which an exclusive property or rights is claimed are defined as follows:

1. A two-level microbridge bolometer imaging array comprising:  
5 an array of bolometer pixels on a semi-conductor substrate,  
each one of said pixels having a lower section on the  
surface of the substrate and a microbridge upper detector  
plane spaced from and immediately above the lower  
section;  
10 said lower section including a semiconductor diode, x and y bus  
lines and x and y pads,  
said microbridge upper detector plane comprising a bridging  
dielectric layer having embedded throughout a  
temperature responsive resistive element having first and  
15 second terminals, said microbridge upper detector plane  
being supported above the lower section by dielectric leg  
portions which are downward extending continuation of  
the bridging dielectric layer;  
said first and second terminals being continued down said leg  
20 portions to said diode and one of said bus lines.
2. The imaging array according to claim 1 wherein said dielectric  
layer is of silicon nitride.
- 25 3. The imaging array according to claim 2 wherein said silicon  
nitride layer comprises a first layer beneath said temperature responsive  
resistive element and a second layer over said first layer and said element.



4. The imaging array according to claim 1 wherein said temperature responsive resistive element is of a nickel-iron alloy.

5. The imaging array according to claim 1 wherein the microbridge upper detector plane is raised about 3 microns above the lower section.

6. The method of fabricating a two-level microbridge bolometer imaging array comprising the steps of:

forming on a silicon substrate a lower level of diodes and other components, column and row bus connectors, and x and y contact pads covered by a first dielectric;

opening contact areas through the first dielectric to one of said bus conductors and to one of said diodes contact areas in each pixel of the array, and to said x and y contact pads at the ends of the bus lines;

coating said first dielectric with a layer of glass;

cutting narrow valleys through the glass along the array column conductors and removing the glass from outside the area of the array, and sloping the edges of the remaining glass ridges to accept further coating;

coating the glass ridges and edges with a first thin film layer of silicon nitride;

opening contact areas through the first layer of silicon nitride to one of said bus conductors, and one of said diodes in each pixel of the array, and to the x and y pads;

patterning on the first layer of silicon nitride on each pixel and between the bus line contact area and the diode contact area on each pixel, a separation path of resistive metal

which has a substantial temperature coefficient of resistance;

adding a second layer of silicon nitride over the first and over the resistive metal path to passify it, said silicon nitride layers forming an elevated plane;

cutting a narrow slit through the silicon nitride to the glass between adjoining pixels, and cutting additional narrow slits in each pixel area to provide further access to the glass, and cutting the nitride from the x and y pad areas; and

dissolving the glass beneath the silicon nitride layers to leave a cavity between the lower level and the elevated plane.

7. The method according to claim 6 wherein said first dielectric is of silicon nitride.

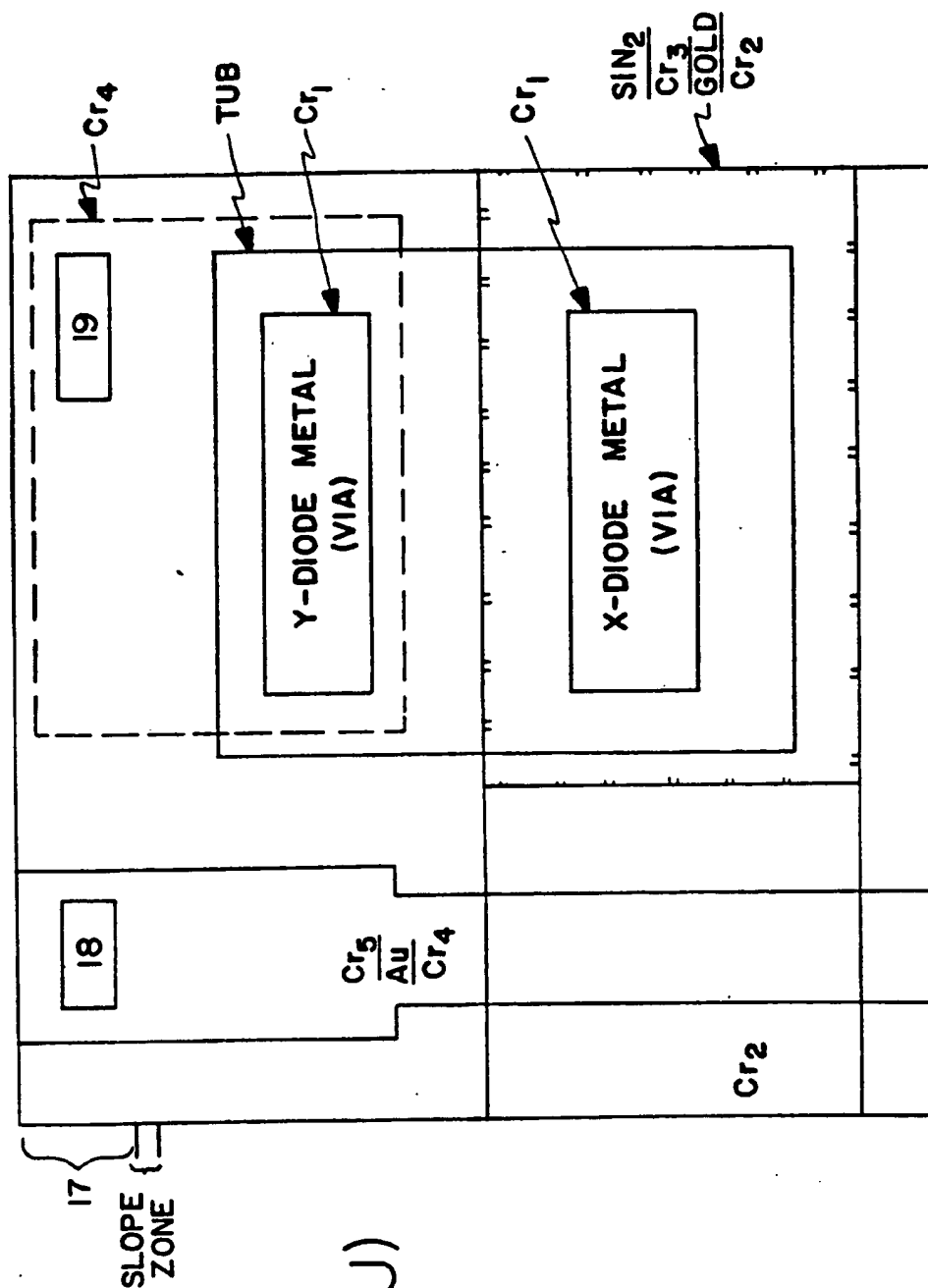
8. The method according to claim 6 wherein the resistive metal is an alloy of nickel-iron.

9. The method according to claim 6 wherein the layer thickness of the glass is about three microns.

10. The method according to claim 6 wherein the cavity is about three microns high.



Fig. 2



(U)

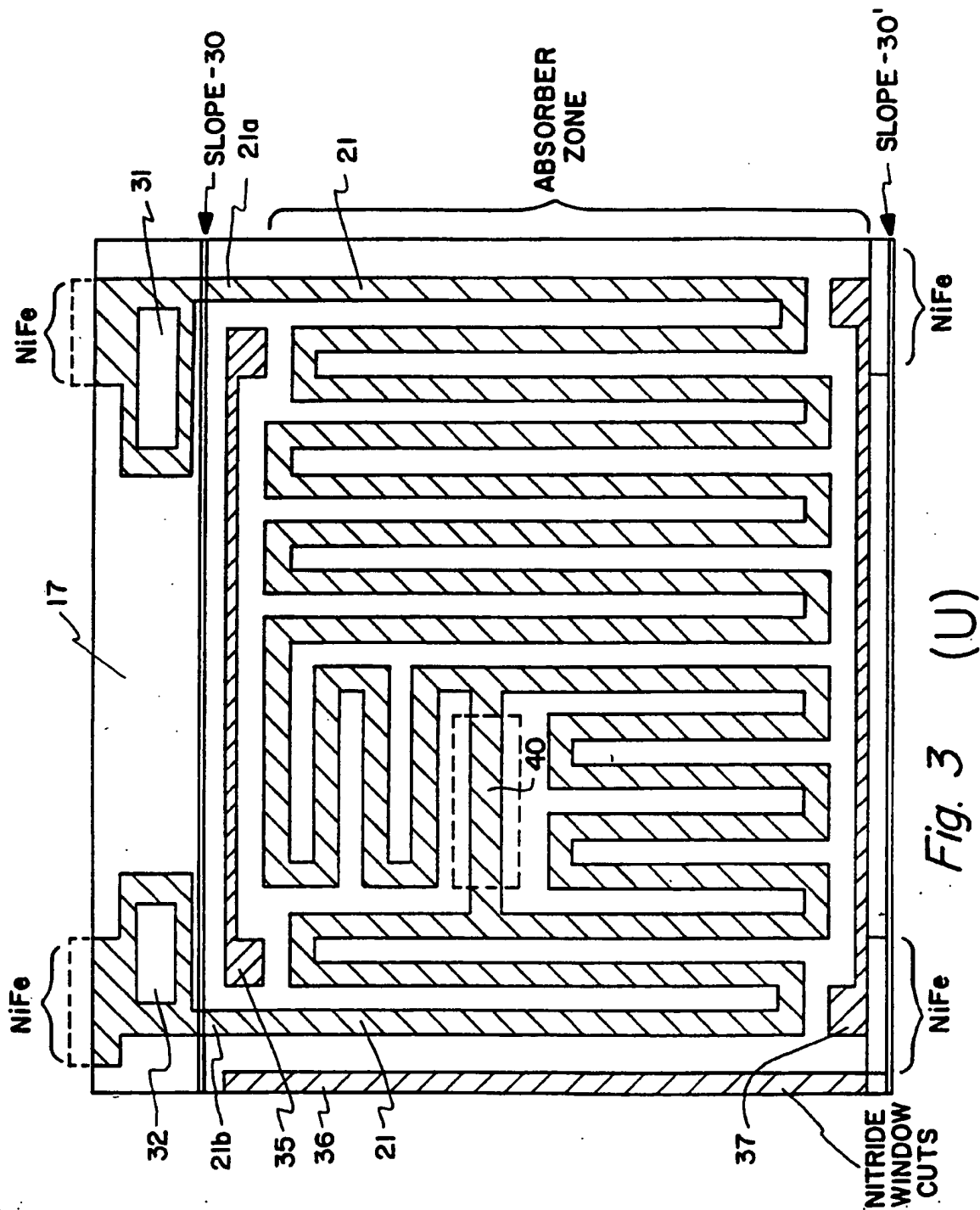
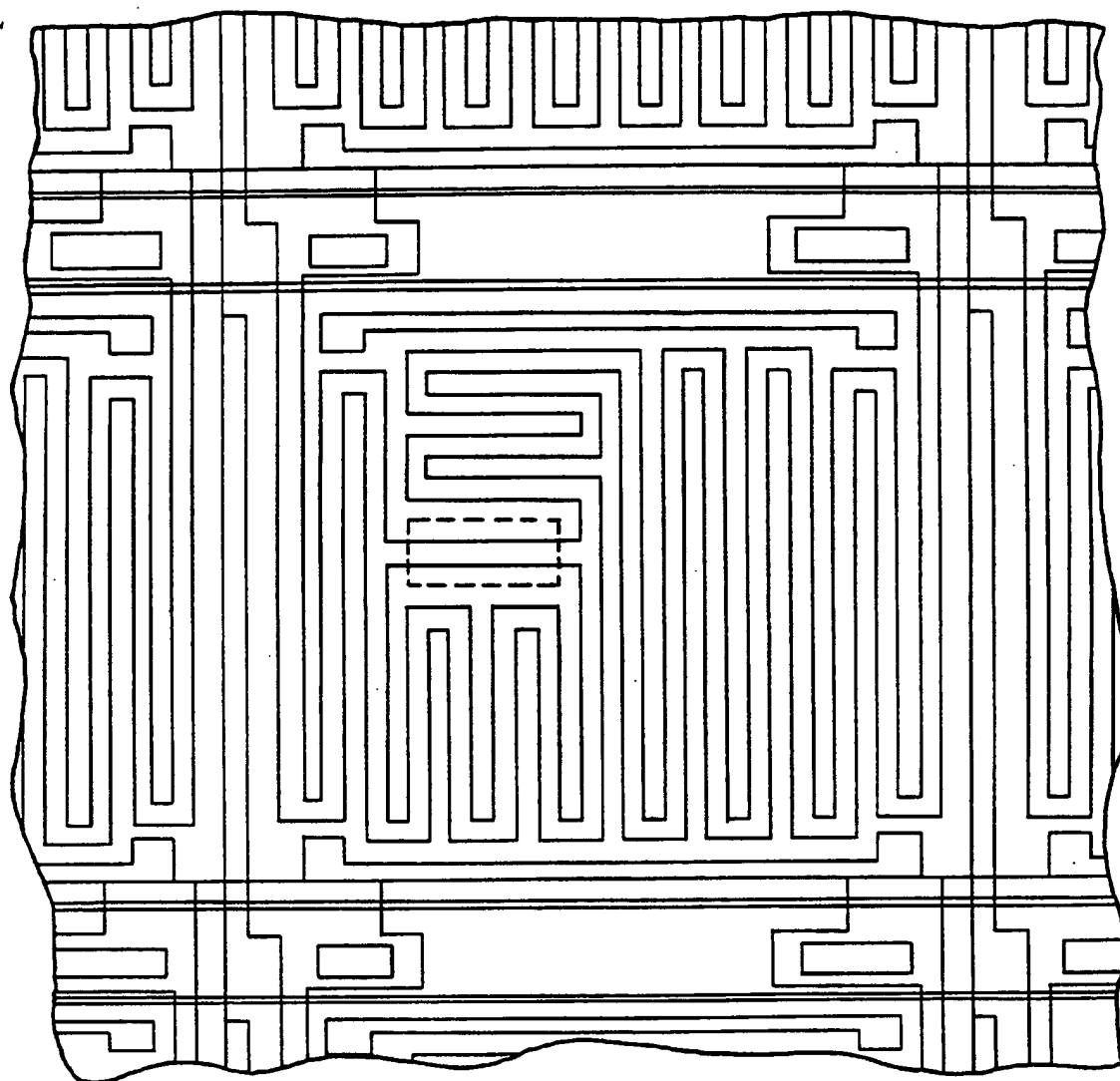


Fig. 3 (U)



*Fig. 3A*

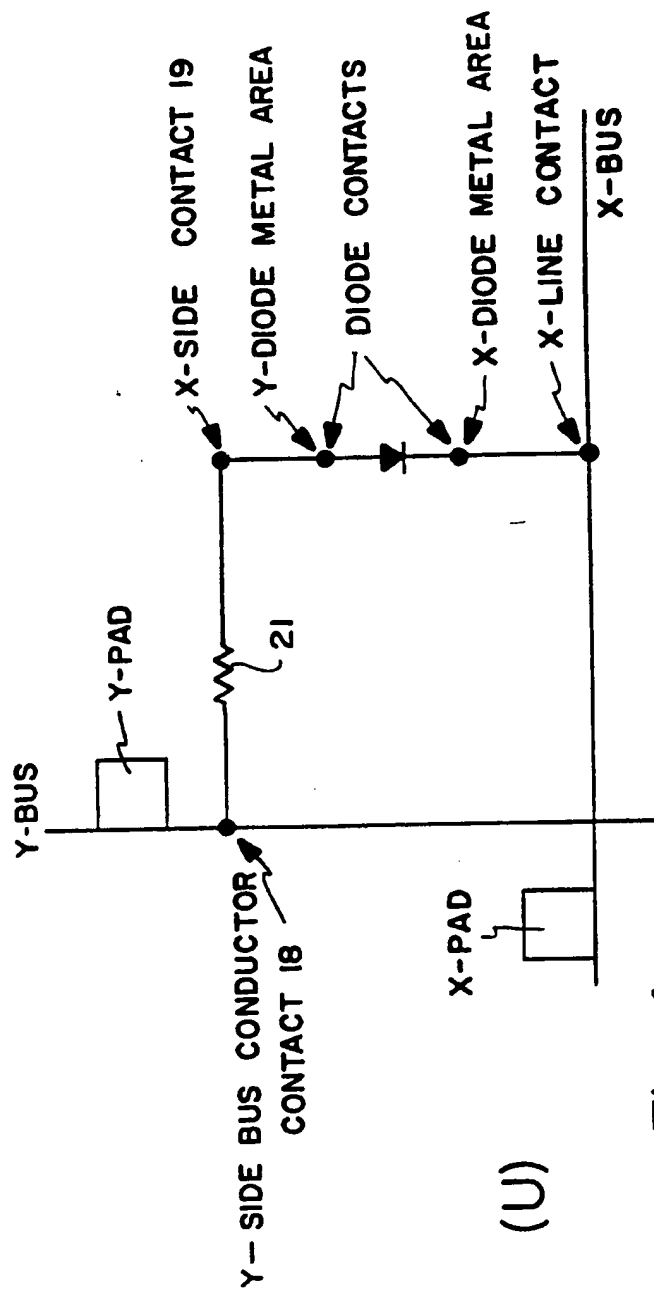


Fig. 4

(U)

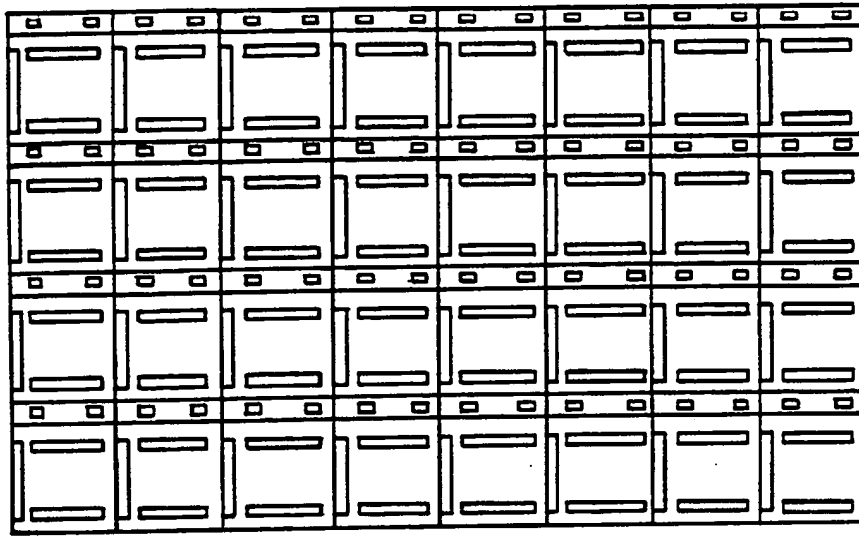


Fig. 6 (U)

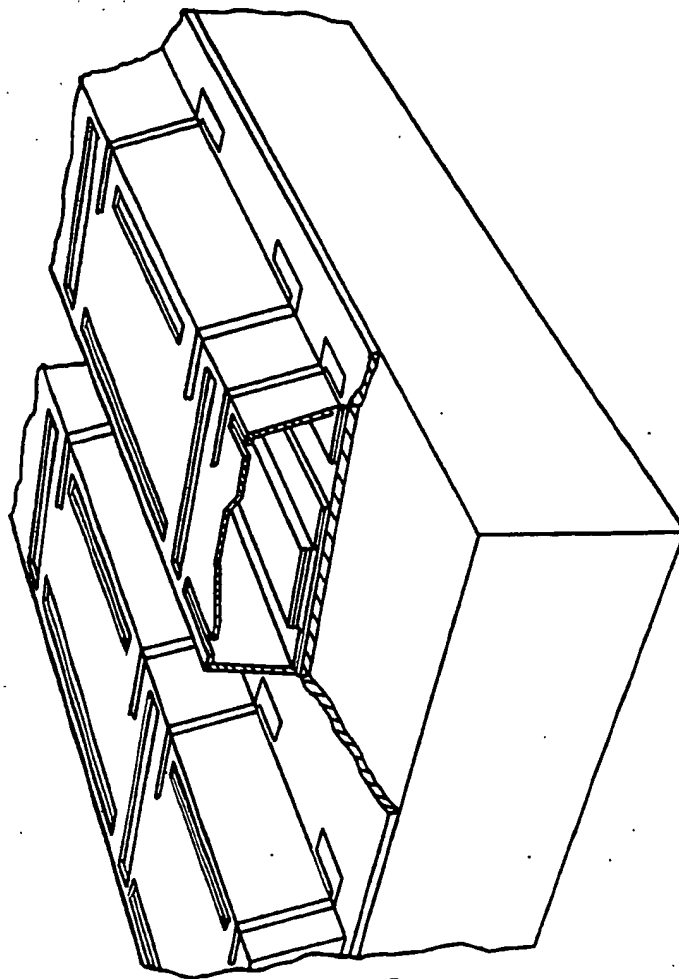


Fig. 5 (U)

SUBSTITUTE SHEET



## INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 92/04895

## A. CLASSIFICATION OF SUBJECT MATTER

IPC5: H01L 31/08, G01J 5/20

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC5: H01L G01J

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO, A1, 9016082 (HUGHES AIRCRAFT COMPANY), 27 December 1990 (27.12.90), page 1, line 3 - line 6; page 8, line 11 - page 11, line 19; page 20, line 4 - line 34; figures 11,21, 22, claims 1,2, abstract, see page 24, line 26 - page 25, line 34.	1
A	--	2-10
A	US, A, 5008541 (AUDAIRE L ET AL), 16 April 1991 (16.04.91), column 3, line 37 - column 6, line 6; figure 4, abstract	1-10
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☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

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**INTERNATIONAL SEARCH REPORT**  
Information on patent family members

08/01/93

International application No.

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO-A1- 9016082	27/12/90	EP-A- 0429566 JP-T- 4500437 US-A- 4922116	05/06/91 23/01/92 01/05/90
US-A- 5008541	16/04/91	EP-A- 0371868 FR-A,B- 2639784 JP-A- 2189971	06/06/90 01/06/90 25/07/90